(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
18 July 2002 (18.07.2002)

PCT

(10) International Publication Number
WO 02/056417 A2

(51) International Patent Classification[7]: H01Q 1/38, C04B 35/117, C30B 29/32

(21) International Application Number: PCT/US01/46906

(22) International Filing Date: 6 December 2001 (06.12.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/758,723 11 January 2001 (11.01.2001) US

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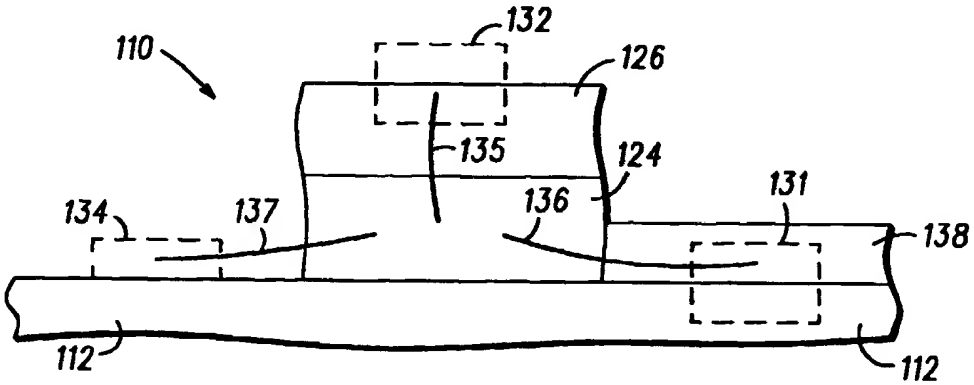
(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *without international search report and to be republished upon receipt of that report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: TUNABLE STRUCTURE UTILIZING A COMPLIANT SUBSTRATE



(57) Abstract: A highly tunable structure (20) can be monolithically integrated upon a monocrystalline semiconductor substrate (22) according to the structure and process described herein. High quality epitaxial layers of monocrystalline materials can be grown overlying monocrystalline substrates (22) such as large silicon wafers by forming a compliant substrate for growing the monocrystalline layers. An amorphous interface layer (28) dissipates strain and permits the growth of a high quality monocrystalline buffer layer (24). In addition, formation of a compliant substrate may include utilizing surfactant enhanced epitaxy (61) and epitaxial growth of Zintl phase materials (130).

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TUNABLE STRUCTURE UTILIZING A COMPLIANT SUBSTRATE

Field of the Invention

This invention relates generally to tunable structures and devices and to a method for their fabrication, and more specifically to an improved tunable structure and to a method for monolithically integrating the tunable structure with silicon devices and circuits.

Background of the Invention

The dielectric constant of tunable structures can be varied (i.e., tuned) by an applied dc (direct current; "bias") electric field. As the material's dielectric constant changes, so does the material's electrical length. This phenomenon has led to using tunable structures as a variable element in tunable microwave devices, such as phase shifters, tunable filters, phase array antennas, and delay lines.

Barium strontium titanate (BSTO) has been known to be used for its high dielectric constant (approximately ranging from 200 to 6,000) in various electronic applications. For example, BSTO has received a great deal of attention as a suitable dielectric material for DRAMs (dynamic random access memories), bypass capacitors, IR detectors, and tunable microwave device applications. In general, BSTO exhibits a high dielectric constant, low dielectric loss, good thermal stability, and good high frequency characteristics. The nonlinearity of its dielectric properties with respect to applied dc voltage makes BSTO especially attractive for tunable microwave devices such as filters, varactors, delay lines, and phase shifters. Thin films of BSTO offer the additional advantages of lightweight, compactness, low processing temperatures, low operating voltages, and compatibility with semiconductor processing technology.

Various attempts have been proposed to combine (dope) BSTO with various other materials and/or compound to further improve its use for electrical applications. For example, bulk composites of BSTO and magnesium oxide (MgO) have been reported to improve the dielectric tunability characteristics and reduce the dielectric loss as compared to pure BSTO. For specific examples reporting the structural and electrical properties of doped BSTO, refer to the following patents and publications: U.S. Patent No. 5,427,988 issued to Sengupta et al. on June 27, 1995 (BSTO-MgO composite); U.S. Patent No. 5,635,433 issued to Sengupta on June 3, 1997 (BSTO-ZnO composite); Joshi et al., "Mg-Doped $Ba_{0.6}Sr_{0.4}TiO_3$ Thin Films For Tunable Microwave Applications," *Applied Physics Letters*, vol 77 num 2, pp. 289-291 (10 July 2000);

Carlson et al., "Large Dielectric Constant (ϵ/ϵ_0 >6000) $Ba_{0.4}Sr_{0.6}TiO_3$ Thin Films For High-Performance Microwave Phase Shifters," *Applied Physics Letters*, vol 76 num 14, pp. 1920-1922 (3 April 2000) (BST/MgO and BST/LAO ($LaAlO_3$).

Semiconductor devices often include multiple layers of conductive, insulating, and semiconductive layers. Often, the desirable properties of such layers improve with the crystallinity of the layer. For example, the electron mobility and band gap of semiconductive layers improves as the crystallinity of the layer increases. Similarly, the free electron concentration of conductive layers and the electron charge displacement and electron energy recoverability of insulative or dielectric films improves as the crystallinity of these layers increases.

For many years, attempts have been made to grow various monolithic thin films on a foreign substrate such as silicon (Si). To achieve optimal characteristics of the various monolithic layers, however, a monocrystalline film of high crystalline quality is desired. Attempts have been made, for example, to grow various monocrystalline layers on a substrate such as germanium, silicon, and various insulators. These attempts have generally been unsuccessful because lattice mismatches between the host crystal and the grown crystal have caused the resulting layer of monocrystalline material to be of low crystalline quality.

If a large area thin film of high quality monocrystalline material was available at low cost, a variety of semiconductor devices could advantageously be fabricated in or using that film at a low cost compared to the cost of fabricating such devices beginning with a bulk wafer of semiconductor material or in an epitaxial film of such material on a bulk wafer of semiconductor material. In addition, if a thin film of high quality monocrystalline material could be realized beginning with a bulk wafer such as a silicon wafer, an integrated device structure, such as an integrated tunable structure or an integrated phase shifter, could be achieved that took advantage of the best properties of both the silicon, the high quality monocrystalline layer, such as BSTO, and the high quality monocrystalline semiconductor layer, such as gallium arsenide.

Accordingly, a need exists for a tunable structure having a high quality monocrystalline film or layer having a changeable dielectric constant over another monocrystalline material suitable for a variety of electrical devices, and for a process for making such a structure. In other words, there is a need for providing the formation of a monocrystalline substrate that is compliant with a high quality monocrystalline material layer so that true two-dimensional growth can be achieved for the formation of quality tunable structures, and semiconductor devices, which are monolithically integrated with silicon-based circuitry.

Brief Description of the Drawings

The present invention is illustrated by way of example and not limitation in the accompanying figures, in which like references indicate similar elements, and in which:

FIGS. 1 and 2 illustrate schematically, in cross section, device structures in accordance with various embodiments of the invention;

FIG. 3 illustrates graphically the relationship between maximum attainable film thickness and lattice mismatch between a host crystal and a grown crystalline overlayer;

FIG. 4 illustrates a high resolution Transmission Electron Micrograph of a structure including a monocrystalline accommodating buffer layer;

FIG. 5 illustrates an x-ray diffraction spectrum of a structure including a monocrystalline accommodating buffer layer;

FIGS. 6A-6D illustrate schematically, in cross-section, the formation of a device structure in accordance with another embodiment of the invention;

FIGS. 7A-7D illustrate a probable molecular bonding structure of the device structures illustrated in FIGS. 6A-6D;

FIGS. 8-10 illustrate schematically, in cross-section, the formation of yet another embodiment of a device structure in accordance with the invention;

FIG. 11 illustrates schematically, in cross-section, a tunable structure in accordance with one embodiment of the invention; and

FIG. 12 illustrates schematically, a phased array antenna system in accordance with embodiment of the invention.

Skilled artisans will appreciate that elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale. For example, the dimensions of some of the elements in the figures may be exaggerated relative to other elements to help to improve understanding of embodiments of the present invention.

Detailed Description of the Drawings

FIG. 1 illustrates schematically, in cross section, a portion of a tunable structure 20 in accordance with an embodiment of the invention. Structure 20 includes a monocrystalline substrate 22, an accommodating buffer layer 24 comprising a monocrystalline material, and a monocrystalline semiconductor layer 26. In this context, the term "monocrystalline" shall have the meaning commonly used within the semiconductor industry. The term shall refer to materials that are a single crystal or that are substantially a single crystal and shall include those

materials having a relatively small number of defects such as dislocations and the like as are commonly found in substrates of silicon or germanium or mixtures of silicon and germanium and epitaxial layers of such materials commonly found in the semiconductor industry.

In accordance with one embodiment of the invention, structure 20 also includes an amorphous intermediate layer 28 positioned between substrate 22 and accommodating buffer layer 24. Structure 20 may also include a template layer 30 between the accommodating buffer layer and monocrystalline semiconductor layer 26. As will be explained more fully below, the template layer helps to initiate the growth of the monocrystalline semiconductor layer on the accommodating buffer layer. The amorphous intermediate layer helps to relieve the strain in the accommodating buffer layer and by doing so, aids in the growth of a high crystalline quality accommodating buffer layer.

Substrate 22, in accordance with an embodiment of the invention, is a monocrystalline semiconductor or compound semiconductor wafer, preferably of large diameter. The wafer may be, for example, a material from Group IV of the periodic table, and preferably a material from Group IVB. Examples of Group IV semiconductor materials include silicon, germanium, mixed silicon and germanium, mixed silicon and carbon, mixed silicon, germanium and carbon, and the like. Preferably substrate 22 is a wafer containing silicon or germanium, and most preferably is a high quality monocrystalline silicon wafer as used in the semiconductor industry.

The material of accommodating buffer layer 24 is preferably selected for its crystalline compatibility with the underlying substrate and with the overlying semiconductor material. Additionally, buffer layer 24 is preferably selected for its tunable properties. Moreover, buffer layer 24 is preferably a monocrystalline oxide or nitride having the characteristics described herein and may include such materials as alkaline earth metal titanates, alkaline earth metal zirconates, alkaline earth metal hafnates, alkaline earth metal tantalates, alkaline earth metal ruthenates, alkaline earth metal niobates, alkaline earth metal vanadates, perovskite oxides such as alkaline earth metal tin-based perovskites, lanthanum aluminate, lanthanum scandium oxide, and gadolinium oxide. Generally, these materials are metal oxides or metal nitrides, and more particularly, these metal oxide or nitrides typically include at least two different metallic elements. In some specific applications, the metal oxides or nitrides may include three or more different metallic elements. Moreover, depending upon the particular application, layer 24 may be a composite of two or more compounds.

The material for monocrystalline semiconductor layer 26 can be selected, as desired, for a particular structure or application, and more particularly, is selected to accommodate one or more electrical devices. For example, the monocrystalline material of layer 26 may comprise a compound semiconductor which can be selected, as needed for a particular semiconductor

structure, from any of the Group IIIA and VA elements (III-V semiconductor compounds), mixed III-V compounds, Group II(A or B) and VIA elements (II-VI semiconductor compounds), and mixed II-VI compounds. Examples include gallium arsenide (GaAs), gallium indium arsenide (GaInAs), gallium aluminum arsenide (GaAlAs), indium phosphide (InP), cadmium sulfide (CdS), cadmium mercury telluride (CdHgTe), zinc selenide (ZnSe), zinc sulfur selenide (ZnSSe), and the like. However, monocrystalline semiconductor layer 26 may also comprise other semiconductor materials, metals, or non-metal materials which are used in the formation of semiconductor structures, devices and/or integrated circuits.

In accordance with one embodiment of the invention, amorphous intermediate layer 28 is grown on substrate 22 at the interface between substrate 22 and the growing accommodating buffer layer. Amorphous intermediate layer 28 is preferably an oxide formed by the oxidation of the surface of substrate 22, and more preferably is composed of a silicon oxide. The thickness of layer 28 is sufficient to relieve strain attributed to mismatches between the lattice constants of substrate 22 and buffer layer 24 (typically in the range of approximately 0.5-5.0 nm). As used herein, lattice constant refers to the distance between atoms of a cell measured in the plane of the surface. If such strain is not relieved by the amorphous intermediate layer, the strain may cause defects in the crystalline structure of the accommodating buffer layer. Defects in the crystalline structure of the accommodating buffer layer, in turn, would make it difficult to achieve a high quality crystalline structure in monocrystalline semiconductor layer 26 which may comprise a semiconductor material, a compound semiconductor material, or another type of material such as a metal or a non-metal.

Appropriate materials for template 30 are discussed below. Suitable template materials chemically bond to the surface of the accommodating buffer layer 24 at selected sites and provide sites for the nucleation of the epitaxial growth of monocrystalline semiconductor layer 26. When used, template layer 30 has a thickness ranging from about 1 to about 10 monolayers.

FIG. 2 illustrates, in cross section, a portion of a semiconductor structure 40 in accordance with a further embodiment of the invention. Structure 40 is similar to the previously described semiconductor structure 20, except that an additional buffer layer 32 is positioned between accommodating buffer layer 24 and monocrystalline semiconductor layer 26. Specifically, the additional buffer layer is positioned between template layer 30 and overlying semiconductor layer 26. The additional buffer layer, preferably formed of a semiconductor or compound semiconductor material when the monocrystalline semiconductor layer 26 comprises a semiconductor or compound semiconductor material, serves to provide a lattice compensation when the lattice constant of the accommodating buffer layer cannot be adequately matched to the overlying monocrystalline semiconductor or compound semiconductor material layer.

Substrate 22 is a monocrystalline substrate such as a monocrystalline silicon or gallium arsenide substrate. The crystalline structure of the monocrystalline substrate is characterized by a lattice constant and by a lattice orientation. In a similar manner, accommodating buffer layer 24 is also a monocrystalline material and the lattice of that monocrystalline material is characterized by a lattice constant and a crystal orientation. The lattice constants of the accommodating buffer layer and the monocrystalline substrate must be closely matched or, alternatively, must be such that upon rotation of one crystal orientation with respect to the other crystal orientation, a substantial match in lattice constants is achieved. In this context the terms "substantially equal" and "substantially matched" mean that there is sufficient similarity between the lattice constants to permit the growth of a high quality crystalline layer on the underlying layer.

FIG. 3 illustrates graphically the relationship of the achievable thickness of a grown crystal layer of high crystalline quality as a function of the mismatch between the lattice constants of the host crystal and the grown crystal. Curve 42 illustrates the boundary of high crystalline quality material. The area to the right of curve 42 represents layers that have a large number of defects. With no lattice mismatch, it is theoretically possible to grow an infinitely thick, high quality epitaxial layer on the host crystal. As the mismatch in lattice constants increases, the thickness of achievable, high quality crystalline layer decreases rapidly. As a reference point, for example, if the lattice constants between the host crystal and the grown layer are mismatched by more than about 2%, monocrystalline epitaxial layers in excess of about 20 nm cannot be achieved.

In accordance with one embodiment of the invention, substrate 22 is a (100) or (111) oriented monocrystalline silicon wafer and accommodating buffer layer 24 is a layer of BSTO. Substantial matching of lattice constants between these two materials is achieved by rotating the crystal orientation of the titanate material by 45° with respect to the crystal orientation of the silicon substrate wafer. The inclusion in the structure of amorphous interface layer 28, a silicon oxide layer in this example, if it is of sufficient thickness, serves to reduce strain in the titanate monocrystalline layer that might result from any mismatch in the lattice constants of the host silicon wafer and the grown titanate layer. As a result, in accordance with an embodiment of the invention, a high quality, thick, monocrystalline BSTO layer is achievable. For among other reasons, this is advantageous because the characteristics of BSTO layer as a phase shifter are affected by the crystallinity of the layer. In general, as the crystallinity of the BSTO is improved, tunability increases.

Layer 26 is a layer of epitaxially grown monocrystalline material and that crystalline material is also characterized by a crystal lattice constant and a crystal orientation. In

accordance with one embodiment of the invention, the lattice constant of layer 26 differs from the lattice constant of substrate 22. To achieve high crystalline quality in this epitaxially grown monocrystalline layer, the accommodating buffer layer must be of high crystalline quality. In addition, in order to achieve high crystalline quality in layer 26, substantial matching between the crystal lattice constant of the host crystal, in this case, the monocrystalline accommodating buffer layer, and the grown crystal is desired. With properly selected materials this substantial matching of lattice constants is achieved as a result of rotation of the crystal orientation of the grown crystal with respect to the orientation of the host crystal. For example, if the grown crystal is gallium arsenide, aluminum gallium arsenide, zinc selenide, or zinc sulfur selenide and the accommodating buffer layer is monocrystalline $Sr_zBa_{1-z}TiO_3$, substantial matching of crystal lattice constants of the two materials is achieved, wherein the crystal orientation of the grown layer is rotated by 45° with respect to the orientation of the host monocrystalline oxide. Similarly, if the host material is a strontium or barium zirconate or a strontium or barium hafnate or barium tin oxide and the compound semiconductor layer is indium phosphide or gallium indium arsenide or aluminum indium arsenide, substantial matching of crystal lattice constants can be achieved by rotating the orientation of the grown crystal layer by 45° with respect to the host oxide crystal. In some instances, a crystalline semiconductor buffer layer between the host oxide and the grown monocrystalline material layer can be used to reduce strain in the grown monocrystalline material layer that might result from small differences in lattice constants. Better crystalline quality in the grown monocrystalline material layer can thereby be achieved.

FIG. 4 is a high resolution Transmission Electron Micrograph (TEM) of semiconductor material manufactured in accordance with one embodiment of the present invention. Single crystal $SrTiO_3$ accommodating buffer layer 24 was grown epitaxially on silicon substrate 22. During this growth process, amorphous interfacial layer 28 is formed which relieves strain due to lattice mismatch. GaAs compound semiconductor layer 26 was then grown epitaxially using template layer 30.

FIG. 5 illustrates an x-ray diffraction spectrum taken on a structure including GaAs monocrystalline layer 26 comprising GaAs grown on silicon substrate 22 using accommodating buffer layer 24. The peaks in the spectrum indicate that both the accommodating buffer layer 24 and GaAs compound semiconductor layer 26 are single crystal and (100) orientated.

The structure illustrated in FIG. 2 can be formed by the process discussed above with the addition of an additional buffer layer deposition step. The buffer layer is formed overlying the template layer before the deposition of the monocrystalline material layer. If the buffer layer is a monocrystalline material comprising a compound semiconductor superlattice, such a superlattice can be deposited, by MBE for example, on the template described above. If instead the buffer

layer is a monocrystalline material layer comprising a layer of germanium, the process above is modified to cap the strontium titanate monocrystalline layer with a final layer of either strontium or titanium and then by depositing germanium to react with the strontium or titanium. The germanium buffer layer can then be deposited directly on this template.

The following non-limiting, illustrative examples illustrate various combinations of materials useful in structures 20 and 40 in accordance with various alternative embodiments of the invention. These examples are merely illustrative, and it is not intended that the invention be limited to these illustrative examples.

Example 1

In accordance with one embodiment of the invention, monocrystalline substrate 22 is a silicon substrate oriented in the (100) direction. The silicon substrate can be, for example, a silicon substrate as is commonly used in making complementary metal oxide semiconductor (CMOS) integrated circuits having a diameter of about 200-300 mm.

In accordance with this embodiment of the invention, accommodating buffer layer 24 is a monocrystalline layer of SrzBa1-zTiO3 where z ranges from 0 to 1. The value of z is selected to obtain one or more lattice constants closely matched to corresponding lattice constants of the subsequently formed semiconductor layer 26. The accommodating buffer layer can have a thickness of about 2 to about 1000 nanometers (nm) and preferably has a thickness of about 100 nm. In general, it is desired to have an accommodating buffer layer thick enough to isolate the semiconductor layer from the substrate to obtain the desired electrical and optical properties.

In accordance with this embodiment of the invention, amorphous intermediate layer 28 is a layer of silicon oxide (SiOx) formed at the interface between the silicon substrate and the accommodating buffer layer. Layer 28 can have a thickness of about 0.5-5 nm, and preferably a thickness of about 1 to 2 nm.

In accordance with this embodiment of the invention, monocrystalline layer 26 is a compound semiconductor layer of gallium arsenide (GaAs) or aluminum gallium arsenide (AlGaAs) having a thickness of about 1 nm to about 100 micrometers (μm) and preferably a thickness of about 0.5 μm to 10 μm. The thickness generally depends on the application for which the layer is being prepared.

To facilitate the epitaxial growth of the gallium arsenide or aluminum gallium arsenide on the monocrystalline oxide, a template layer is formed by capping the oxide layer. The template layer is preferably 1-10 monolayers of Ti-As, Sr-O-As, Sr-Ga-O, or Sr-Al-O. By way

of a preferred example, 1-2 monolayers of Ti-As or Sr-Ga-O have been shown to successfully grow GaAs layers.

Example 2

This embodiment of the invention is an example of structure 40 illustrated in FIG. 2. Substrate 22, accommodating buffer layer 24, and monocrystalline semiconductor layer 26 can be similar to those described in example 1.

In addition, an additional buffer layer 32 serves to alleviate any strains that might result from a mismatch of the crystal lattice of the accommodating buffer layer and the lattice of the monocrystalline semiconductor material. Buffer layer 32 can be a layer of germanium or GaAs, an aluminum gallium arsenide (AlGaAs), an indium gallium phosphide (InGaP), an aluminum gallium phosphide (AlGaP), an indium gallium arsenide (InGaAs), an aluminum indium phosphide (AlInP), a gallium arsenide phosphide (GaAsP), or an indium gallium phosphide (InGaP) strain compensated superlattice. In accordance with one aspect of this embodiment, buffer layer 32 includes a $GaAs_xP_{1-x}$ superlattice, wherein the value of x ranges from 0 to 1.

In accordance with another aspect, buffer layer 32 includes an $In_yGa_{1-y}P$ superlattice, wherein the value of y ranges from 0 to 1. By varying the value of x or y, as the case may be, the lattice constant is varied from bottom to top across the superlattice to create a match between lattice constants of the underlying oxide and the overlying monocrystalline material which in this example is a compound semiconductor material. The compositions of other compound semiconductor materials, such as those listed above, may also be similarly varied to manipulate the lattice constant of layer 32 in a like manner. The superlattice can have a thickness of about 50-500 nm and preferably has a thickness of about 100-200 nm.

Alternatively, buffer layer 32 can be a layer of monocrystalline germanium having a thickness of 1-50 nm and preferably having a thickness of about 2-20 nm. In using a germanium buffer layer, a template layer of either germanium-strontium (Ge-Sr) or germanium-titanium (Ge-Ti) having a thickness of about one monolayer can be used as a nucleating site for the subsequent growth of the monocrystalline material layer which in this example is a compound semiconductor material. The formation of the oxide layer is capped with either a monolayer of strontium or a monolayer of titanium to act as a nucleating site for the subsequent deposition of the monocrystalline germanium. The monolayer of strontium or titanium provides a nucleating site to which the first monolayer of germanium can bond.

The template for this structure can be the same of that described in Example 1.

Example 3

This example also illustrates materials useful in a structure 40 as illustrated in FIG. 2. Substrate material 22, accommodating buffer layer 24, monocrystalline material layer 26 and template layer 30.

In addition, additional buffer layer 32 is inserted between the accommodating buffer layer and the overlying monocrystalline material layer. Buffer layer 32, a further monocrystalline material which in this instance comprises a semiconductor material can be, for example, a graded layer of indium gallium arsenide (InGaAs) or indium aluminum arsenide (InAlAs). In accordance with one aspect of this embodiment, additional buffer layer 32 includes InGaAs, in which the indium composition varies from 0 to about 50%. The buffer layer preferably has a thickness of about 10-30 nm. Varying the composition of the buffer layer from GaAs to InGaAs serves to provide a lattice match between the underlying monocrystalline oxide material and the overlying layer of monocrystalline material which in this example is a compound semiconductor material. Such a buffer layer is especially advantageous if there is a lattice mismatch between accommodating buffer layer 24 and monocrystalline material layer 26.

The following example illustrates a process, in accordance with one embodiment of the invention, for fabricating a tunable structure such as the structures depicted in FIGS. 1 and 2. The process starts by providing a monocrystalline semiconductor substrate comprising silicon or germanium. In accordance with a preferred embodiment of the invention, the semiconductor substrate is a silicon wafer having a (100) orientation. The substrate is preferably oriented on axis or, at most, about 4° off axis. At least a portion of the semiconductor substrate has a bare surface, although other portions of the substrate, as described below, may encompass other structures. The term "bare" in this context means that the surface in the portion of the substrate has been cleaned to remove any oxides, contaminants, or other foreign material. As is well known, bare silicon is highly reactive and readily forms a native oxide. The term "bare" is intended to encompass such a native oxide. A thin silicon oxide may also be intentionally grown on the semiconductor substrate, although such a grown oxide is not essential to the process in accordance with the invention. In order to epitaxially grow a monocrystalline oxide layer overlying the monocrystalline substrate, the native oxide layer must first be removed to expose the crystalline structure of the underlying substrate. The following process is preferably carried out by molecular beam epitaxy (MBE), although other epitaxial processes may also be used in accordance with the present invention. The native oxide can be removed by first thermally depositing a thin layer of strontium, barium, a combination of strontium and barium, or other

alkali earth metals or combinations of alkali earth metals in an MBE apparatus. In the case where strontium is used, the substrate is then heated to a temperature of about 850° C to cause the strontium to react with the native silicon oxide layer. The strontium serves to reduce the silicon oxide to leave a silicon oxide-free surface. The resultant surface, which exhibits an ordered 2x1 structure, includes strontium, oxygen, and silicon. The ordered 2x1 structure forms a template for the ordered growth of an overlying layer of a monocrystalline oxide. The template provides the necessary chemical and physical properties to nucleate the crystalline growth of an overlying layer.

In accordance with an alternate embodiment of the invention, the native silicon oxide can be converted and the substrate surface can be prepared for the growth of a monocrystalline oxide layer by depositing an alkali earth metal oxide, such as strontium oxide, strontium barium oxide, or barium oxide, onto the substrate surface by MBE at a low temperature and by subsequently heating the structure to a temperature of about 850°C. At this temperature a solid state reaction takes place between the strontium oxide and the native silicon oxide causing the reduction of the native silicon oxide and leaving an ordered 2x1 structure with strontium, oxygen, and silicon remaining on the substrate surface. Again, this forms a template for the subsequent growth of an ordered monocrystalline oxide layer.

Following the removal of the silicon oxide from the surface of the substrate, in accordance with one embodiment of the invention, the substrate is cooled to a temperature in the range of about 200-800°C and a layer of strontium titanate is grown on the template layer by molecular beam epitaxy. The MBE process is initiated by opening shutters in the MBE apparatus to expose strontium, titanium and oxygen sources. The ratio of strontium and titanium is approximately 1:1. The partial pressure of oxygen is initially set at a minimum value to grow stochiometric strontium titanate at a growth rate of about 0.3-0.5 nm per minute. After initiating growth of the strontium titanate, the partial pressure of oxygen is increased above the initial minimum value. The overpressure of oxygen causes the growth of an amorphous silicon oxide layer at the interface between the underlying substrate and the growing strontium titanate layer. The growth of the silicon oxide layer results from the diffusion of oxygen through the growing strontium titanate layer to the interface where the oxygen reacts with silicon at the surface of the underlying substrate. The strontium titanate grows as an ordered monocrystal with the crystalline orientation rotated by 45° with respect to the ordered 2x1 crystalline structure of the underlying substrate. Strain that otherwise might exist in the strontium titanate layer because of the small mismatch in lattice constant between the silicon substrate and the growing crystal is relieved in the amorphous silicon oxide intermediate layer.

After the strontium titanate layer has been grown to the desired thickness, the monocrystalline strontium titanate is capped by a template layer that is conducive to the subsequent growth of an epitaxial layer of a desired monocrystalline material. For example, for the subsequent growth of a monocrystalline compound semiconductor material layer of gallium arsenide, the MBE growth of the strontium titanate monocrystalline layer can be capped by terminating the growth with 1-2 monolayers of titanium, 1-2 monolayers of titanium-oxygen or with 1-2 monolayers of strontium-oxygen. Following the formation of this capping layer, arsenic is deposited to form a Ti-As bond, a Ti-O-As bond or a Sr-O-As. Any of these form an appropriate template for deposition and formation of a gallium arsenide monocrystalline layer. Following the formation of the template, gallium is subsequently introduced to the reaction with the arsenic and gallium arsenide forms. Alternatively, gallium can be deposited on the capping layer to form a Sr-O-Ga bond, and arsenic is subsequently introduced with the gallium to form the GaAs.

The process described above illustrates a process for forming a semiconductor structure including a silicon substrate, an overlying oxide layer, and a monocrystalline material layer comprising a gallium arsenide compound semiconductor layer by the process of molecular beam epitaxy. The process can also be carried out by the process of chemical vapor deposition (CVD), metal organic chemical vapor deposition (MOCVD), migration enhanced epitaxy (MEE), atomic layer epitaxy (ALE), physical vapor deposition (PVD), chemical solution deposition (CSD), pulsed laser deposition (PLD), or the like. Further, by a similar process, other monocrystalline accommodating buffer layers such as alkaline earth metal titanates, zirconates, hafnates, tantalates, vanadates, ruthenates, and niobates, peroskite oxides such as alkaline earth metal tin-based perovskites, lanthanum aluminate, lanthanum scandium oxide, and gadolinium oxide can also be grown. Further, by a similar process such as MBE, other monocrystalline material layers comprising other III-V and II-VI monocrystalline compound semiconductors, semiconductors, metals and non-metals can be deposited overlying the monocrystalline oxide accommodating buffer layer.

Each of the variations of monocrystalline material layer and monocrystalline oxide accommodating buffer layer uses an appropriate template for initiating the growth of the monocrystalline material layer. For example, if the accommodating buffer layer is an alkaline earth metal zirconate, the oxide can be capped by a thin layer of zirconium. The deposition of zirconium can be followed by the deposition of arsenic or phosphorus to react with the zirconium as a precursor to depositing indium gallium arsenide, indium aluminum arsenide, or indium phosphide respectively. Similarly, if the monocrystalline oxide accommodating buffer layer is an alkaline earth metal hafnate, the oxide layer can be capped by a thin layer of hafnium.

The deposition of hafnium is followed by the deposition of arsenic or phosphorous to react with the hafnium as a precursor to the growth of an indium gallium arsenide, indium aluminum arsenide, or indium phosphide layer, respectively. In a similar manner, strontium titanate can be capped with a layer of strontium or strontium and oxygen and barium titanate can be capped with a layer of barium or barium and oxygen. Each of these depositions can be followed by the deposition of arsenic or phosphorus to react with the capping material to form a template for the deposition of a monocrystalline material layer comprising compound semiconductors such as indium gallium arsenide, indium aluminum arsenide, or indium phosphide.

FIGS. 6A-6D illustrate schematically, in cross section, the formation of a tunable structure 50 in accordance with another embodiment of the invention. Like the previously described embodiments referred to in FIGS. 1 and 2, this embodiment of the invention involves the process of forming a compliant substrate utilizing the epitaxial growth of single crystal oxides, such as the formation of accommodating buffer layer 24 previously described with reference to FIGS. 1 and 2 and the formation of a template layer 30. However, the embodiment illustrated in FIGS. 6A-6D utilizes a template that includes a surfactant to facilitate layer-by-layer monocrystalline material growth.

Turning now to FIG. 6A, an amorphous intermediate layer 58 is grown on substrate 52 at the interface between substrate 52 and a growing accommodating buffer layer 54, which is preferably a monocrystalline crystal oxide layer, by the oxidation of substrate 52 during the growth of layer 54. Layer 54 is preferably a monocrystalline oxide material such as a monocrystalline layer of $Sr_zBa_{1-z}TiO_3$ where z ranges from 0 to 1. However, layer 54 may also comprise any of those compounds previously described with reference layer 24 in FIGS. 1-2.

Layer 54 is grown with a strontium (Sr) terminated surface represented in FIG. 6A by hatched line 55 which is followed by the addition of a template layer 60 which includes a surfactant layer 61 and capping layer 63 as illustrated in FIGS. 6B and 6C. Surfactant layer 61 may comprise, but is not limited to, elements such as Al, In and Ga, but will be dependent upon the composition of layer 54 and the overlying layer of monocrystalline material for optimal results. In one exemplary embodiment, aluminum (Al) is used for surfactant layer 61 and functions to modify the surface and surface energy of layer 54. Preferably, surfactant layer 61 is epitaxially grown, to a thickness of one to two monolayers, over layer 54 as illustrated in FIG. 6B by way of molecular beam epitaxy (MBE), although other epitaxial processes may also be performed including chemical vapor deposition (CVD), metal organic chemical vapor deposition (MOCVD), migration enhanced epitaxy (MEE), atomic layer epitaxy (ALE), physical vapor deposition (PVD), chemical solution deposition (CSD), pulsed laser deposition (PLD), or the like.

Surfactant layer 61 is then exposed to a halogen such as arsenic, for example, to form capping layer 63 as illustrated in FIG. 6C. Surfactant layer 61 may be exposed to a number of materials to create capping layer 63 such as elements which include, but are not limited to, As, P, Sb and N. Surfactant layer 61 and capping layer 63 combine to form template layer 60.

Monocrystalline semiconductor layer 66, which in this example is a compound semiconductor such as GaAs, is then deposited via MBE, CVD, MOCVD, MEE, ALE, PVD, CSD, PLD, and the like to form the final structure illustrated in FIG. 9D.

FIGS. 7A-7D illustrate possible molecular bond structures for a specific example of compound semiconductor structure 50 formed in accordance with the embodiment of the invention illustrated in FIGS. 6A-6D. More specifically, FIGS. 7A-7D illustrate the growth of GaAs (layer 66) on the strontium terminated surface of a strontium titanate monocrystalline oxide (layer 54) using a surfactant containing template (layer 60).

The growth of a monocrystalline material layer 66 such as GaAs on an accommodating buffer layer 54 such as a strontium titanium oxide over amorphous interface layer 58 and substrate layer 52, both of which may comprise materials previously described with reference to layers 28 and 22, respectively in FIGS. 1 and 2, illustrates a critical thickness of about 1000 Angstroms where the two-dimensional (2D) and three-dimensional (3D) growth shifts because of the surface energies involved. In order to maintain a true layer by layer growth (Frank Van der Mere growth), the following relationship must be satisfied:

$$\delta_{STO} > (\delta_{INT} + \delta_{GaAs})$$

where the surface energy of the monocrystalline oxide layer 54 must be greater than the surface energy of the amorphous interface layer 58 added to the surface energy of the GaAs layer 66.

Since it is impracticable to satisfy this equation, a surfactant containing template was used, as described above with reference to FIGS. 6B-6D, to increase the surface energy of the monocrystalline oxide layer 54 and also to shift the crystalline structure of the template to a diamond-like structure that is in compliance with the original GaAs layer.

FIG. 7A illustrates the molecular bond structure of a strontium terminated surface of a strontium titanate monocrystalline oxide layer. An aluminum surfactant layer is deposited on top of the strontium terminated surface and bonds with that surface as illustrated in FIG. 7B, which reacts to form a capping layer comprising a monolayer of Al_2Sr having the molecular bond structure illustrated in FIG. 7B which forms a diamond-like structure with an sp^3 hybrid terminated surface that is compliant with compound semiconductors such as GaAs. The structure is then exposed to As to form a layer of AlAs as shown in FIG. 7C. GaAs is then deposited to complete the molecular bond structure illustrated in FIG. 7D which has been

obtained by 2D growth. The GaAs can be grown to any thickness for forming other semiconductor structures, devices, or integrated circuits. Alkaline earth metals such as those in Group IIA are those elements preferably used to form the capping surface of the monocrystalline oxide layer 24 because they are capable of forming a desired molecular structure with aluminum.

In this embodiment, a surfactant containing template layer aids in the formation of a compliant substrate for the monolithic integration of various material layers including those comprised of Group III-V compounds to form high quality semiconductor structures, devices and integrated circuits.

FIGS. 8-10 illustrate schematically, in cross-section, the formation of a tunable structure 100 in accordance with yet another embodiment of the invention. This embodiment includes a compliant layer that functions as a transition layer that uses clathrate or Zintl type bonding. More specifically, structure 100 includes an intermetallic template layer to reduce the surface energy of the interface between material layers thereby allowing for two dimensional layer by layer growth.

Structure 100 illustrated in FIG. 8 includes a monocrystalline substrate 102, an amorphous interface layer 108 and an accommodating buffer layer 104. Amorphous intermediate layer 108 is grown on substrate 102 at the interface between substrate 102 and accommodating buffer layer 104 as previously described with reference to FIGS. 1 and 2. Amorphous interface layer 108 may comprise any of those materials previously described with reference to amorphous interface layer 28 in FIGS. 1 and 2 but preferably comprises a monocrystalline oxide material such as a monocrystalline layer of $Sr_zBa_{1-z}TiO_3$ where z ranges from 0 to 1. Substrate 102 is preferably silicon but may also comprise any of those materials previously described with reference to substrate 22.

A template layer 130 is deposited over accommodating buffer layer 104, as illustrated in FIG. 9, and preferably comprises a thin layer of Zintl type phase material composed of metals and metalloids having a great deal of ionic character. As in previously described embodiments, template layer 130 is deposited by way of MBE, CVD, MOCVD, MEE, ALE, PVD, CSD, PLD, or the like to achieve a thickness of one monolayer. Template layer 130 functions as a "soft" layer with non-directional bonding but high crystallinity which absorbs stress build up between layers having lattice mismatch. Materials for template 130 may include, but are not limited to, materials containing Si, Ga, In, and Sb such as, for example, $AlSr_2$, $(MgCaYb)Ga_2$, $(Ca,Sr,Eu,Yb)In_2$, $BaGe_2As$, and $SrSn_2As_2$

A monocrystalline material layer 126 is epitaxially grown over template layer 130 to achieve the final structure illustrated in FIG. 10. As a specific example, an $SrAl_2$ layer may be used as template layer 130 and an appropriate monocrystalline material layer 126 such as a

compound semiconductor material GaAs is grown over the $SrAl_2$. The Al-Ti (from the accommodating buffer layer of layer of $Sr_zBa_{1-z}TiO_3$ where z ranges from 0 to 1) bond is mostly metallic while the Al-As (from the GaAs layer) bond is weakly covalent. The Sr participates in two distinct types of bonding with part of its electric charge going to the oxygen atoms in the lower accommodating buffer layer 104 comprising $Sr_zBa_{1-z}TiO_3$ to participate in ionic bonding and the other part of its valence charge being donated to Al in a way that is typically carried out with Zintl phase materials. The amount of the charge transfer depends on the relative electronegativity of elements comprising the template layer 130 as well as on the interatomic distance. In this example, Al assumes an sp^3 hybridization and can readily form bonds with monocrystalline material layer 126, which in this example, comprises compound semiconductor material GaAs.

The compliant substrate produced by use of the Zintl type template layer used in this embodiment can absorb a large strain without a significant energy cost. In the above example, the bond strength of the Al is adjusted by changing the volume of the $SrAl_2$ layer thereby making the device tunable for specific applications which include the monolithic integration of III-V and Si devices and the monolithic integration of high-k dielectric materials for CMOS technology.

FIG. 11 illustrates schematically, in cross section, a portion of a tunable structure 110 in accordance with an embodiment of the invention. Structure 110 is similar to the previously described structures, in that structure 110 includes a monocrystalline semiconductor substrate 112, a monocrystalline buffer layer 124, and a monocrystalline semiconductor layer 126. In addition, tunable structure 110 may be formed by any one of the previously described embodiments of FIGS. 1-10. Semiconductor substrate 112 may include any of the previously described materials suitable for use in a tunable structure, such as a monocrystalline silicon wafer.

Buffer layer 124 includes a material suitable for use in the tunable structure, and may include any of the previously described materials. In one particular embodiment, layer 124 includes barium strontium titanate (BSTO), due in part, because of several favorable characteristics of BSTO (e.g., low dielectric loss, good high frequency characteristics, good thermal stability).

In one aspect of the present embodiment, BSTO layer 124 may be doped with a suitable material to further improve the tunablility or phase shifting properties. For example, magnesium oxide (MgO) may be combined with BSTO for use in applications including, but not limited to, various antenna systems at both microwave and millimeter wave range frequencies.

In another aspect of the present embodiment, BSTO layer 124 may be doped with zinc oxide (ZnO) for use in applications including, but not limited to, multilayer capacitors, capacitor-varistors, non-volatile computer memory and phased array antenna systems.

It should be appreciated that layer 124, and in this particular embodiment, BSTO layer 124 may be pure or doped depending upon the desired application. Moreover, various other materials may be used as dopants with BSTO aside from MgO and ZnO. For example, among some of the other materials which may be combined with BSTO include, but not limited to, zirconia, alumina, and silicon dioxide.

Semiconductor layer 126 includes a suitable semiconductor material for use in the tunable structure, and may include any of the previously described materials. In one particular embodiment, layer 126 is suitably a layer of Group III-V compound semiconductor material such as GaAs.

Structure 110 further includes one or more electrical devices schematically illustrated by dashed lines 131, 132 and 134. An electrical device generally indicated by the dashed line 131 is formed at least partially in substrate 112. Electrical device 131 can be a resistor, a capacitor, an active semiconductor component such as a diode or a transistor or an integrated logic element or circuit such as a CMOS integrated circuit and formed by conventional semiconductor processing as is well known and widely practiced in the industry. Electrical device 131 may be, for example, a circuit to control the supply of dc to the tunable structure.

A semiconductor device 132 is formed at least partially in compound semiconductor layer 126. Semiconductor device 132 can be formed by processing steps conventionally used in fabrication of GaAs or other suitable compound semiconductor material devices. Device 132 is preferably an active component, such as a device to generate an RF signal. A conductor schematically indicated by lines 135, 136 and 237 can be formed to electrically couple devices 131, 132 and 134 to phase shifting layer 124. Thus, a fully integrated tunable structure is implemented that includes at least one component formed in the monocrystalline compound semiconductor layer and components formed in the silicon substrate.

Another electrical device generally indicated by dashed line 134 is formed on substrate 112 using conventional silicon device processing techniques. Alternatively, device 134 may be formed on semiconductor layer 126. Device 134 may include any suitable input/output element, such as an antenna or the like.

A layer of insulating material 138 such as a layer of silicon dioxide or the like may overlie electrical component 131 to, for example, protect the underlying component from the environment and avoid short circuiting within the structure. It should be noted that a similar insulating material layer may overlie electrical devices 132 and 134 as well.

In practice, a electromagnetic wave (typically high frequency) is generated in RF element 132 and is coupled to layer 124. The wave travels through layer 124 at a speed determined by the dielectric constant of the medium, e.g., BSTO or doped BSTO. The dielectric constant of the material may be changed or altered by an applied dc voltage generated by a digital circuit 131. As the dielectric constant changes, the electrical length of the material changes. Thus, as the wave travels through layer 124, the phase of the wave can be effectively changed (shifted). A suitable input/output component 134, such as an antenna, may be coupled to layer 124 to receive/transmit the phase shifted wave.

FIG. 12 illustrates an exemplary arrangement of a phased array antenna system 140 having a plurality of tunable structures 145 in accordance with the invention. Row and column driver circuits 150 and 152 control the dc voltage to the phase shift elements and steer the antenna radiation pattern. System 140 may be useful in a variety of applications, e.g., antenna tracking.

Clearly, those embodiments specifically describing structures having compound semiconductor portions and Group IV semiconductor portions, are meant to illustrate embodiments of the present invention and not limit the present invention. There are a multiplicity of other combinations and other embodiments of the present invention. For example, the present invention includes structures and methods for fabricating material layers which form semiconductor structures, devices and integrated circuits including other layers such as metal and non-metal layers. More specifically, the invention includes structures and methods for forming a compliant substrate which is used in the fabrication of semiconductor structures, devices and integrated circuits and the material layers suitable for fabricating those structures, devices, and integrated circuits. By using embodiments of the present invention, it is now simpler to integrate devices that include monocrystalline layers comprising semiconductor and compound semiconductor materials as well as other material layers that are used to form those devices with other components that work better or are easily and/or inexpensively formed within semiconductor or compound semiconductor materials. This allows a device to be shrunk, the manufacturing costs to decrease, and yield and reliability to increase.

In the foregoing specification, the invention has been described with reference to specific embodiments. However, one of ordinary skill in the art appreciates that various modifications and changes can be made without departing from the scope of the present invention as set forth in the claims below. Accordingly, the specification and figures are to be regarded in an illustrative rather than a restrictive sense, and all such modifications are intended to be included within the scope of present invention.

Benefits, other advantages, and solutions to problems have been described above with regard to specific embodiments. However, the benefits, advantages, solutions to problems, and any element(s) that may cause any benefit, advantage, or solution to occur or become more pronounced are not to be construed as a critical, required, or essential features or elements of any or all the claims. As used herein, the terms "comprises," "comprising," or any other variation thereof, are intended to cover a non-exclusive inclusion, such that a process, method, article, or apparatus that comprises a list of elements does not include only those elements but may include other elements not expressly listed or inherent to such process, method, article, or apparatus.

We Claim:

1. A phase tunable structure comprising:

a monocrystalline substrate;

a monocrystalline layer formed on the substrate, the layer comprising a material having a tunable dielectric constant;

a template formed on the layer;

a monocrystalline semiconductor material formed overlying the template;

an active semiconductor device formed at least partially in the monocrystalline semiconductor material and coupled to the monocrystalline layer; and

an electrical device formed at least partially in the substrate and coupled to the monocrystalline layer.

2. The phase tunable structure of claim 1 wherein the template comprises a Zintl type phase material.

3. The phase tunable structure of claim 2 wherein the Zintl type phase material comprises at least one of $SrAl_2$, $(MgCaYb)Ga_2$, $(Ca,Sr,Eu,Yb)In_2$, $BaGe_2As$, and $SrSn_2As_2$.

4. The phase tunable structure of claim 1 wherein the layer comprises $Sr_zBa_{1-z}TiO_3$ where z ranges from 0 to 1, the template comprises $SrAl_2$, and the monocrystalline material layer comprises GaAs.

5. The phase tunable structure of claim 1 wherein the template comprises a surfactant material.

6. The phase tunable structure of claim 5 wherein the surfactant comprises at least one of Al, In, and Ga.

7. The phase tunable structure of claim 5 wherein the template further comprises a capping layer.

8. The phase tunable structure of claim 7 wherein the capping layer is formed by exposing the surfactant material to a cap inducing material.

9. The phase tunable structure of claim 7 wherein the cap inducing material comprises at least one of As, P, Sb, and N.

10. The phase tunable structure of claim 7 wherein the surfactant comprises Al, the capping layer comprises Al_2Sr, and the monocrystalline material layer comprises GaAs.

11. The phase tunable structure of claim 1 wherein the template comprises a silicon layer.

12. The phase tunable structure of claim 11 further comprising a capping layer.

13. The phase tunable structure of claim 1 further comprising an input/output device electrically coupled to the monocrystalline layer.

14. The phase tunable structure of claim 13 wherein said input/output device comprises an antenna.

15. The phase tunable structure of claim 1 wherein the layer comprises an oxide selected from the group consisting of alkaline earth metal titanates, alkaline earth metal zirconates, alkaline earth metal hafnates, alkaline earth metal tantalates, alkaline earth metal ruthenates, and alkaline earth metal niobates.

16. The phase tunable structure of claim 1 wherein the layer comprises a doped $Sr_zBa_{1-z}TiO_3$ where z ranges from 0 to 1.

17. The phase tunable structure of claim 16 wherein the layer comprises a BSTO-MgO composite.

18. The phase tunable structure of claim 17 wherein the monocrystalline substrate comprises a Group IV material characterized by a first lattice constant and the monocrystalline semiconductor material is characterized by a second lattice constant different than the first lattice constant.

19. The phase tunable structure of claim 18 wherein the monocrystalline oxide is characterized by a third lattice constant different than the second lattice constant.

20. The phase tunable structure of claim 17 wherein the monocrystalline Group IV substrate is characterized by a first crystalline orientation and the monocrystalline oxide is characterized by a second crystalline orientation and wherein the second crystalline orientation is rotated with respect to the first crystalline orientation.

21. The phase tunable structure of claim 17 further comprising a second amorphous oxide layer formed between the Group IV substrate and the monocrystalline oxide.

22. The phase tunable structure of claim 21 wherein the Group IV substrate comprises silicon and the second amorphous oxide layer comprises a silicon oxide.

23. The phase tunable structure of claim 1 wherein the monocrystalline semiconductor material layer is a compound semiconductor material selected from the group consisting of: III-V compounds, mixed III-V compounds, II-VI compounds, and mixed II-VI compounds.

24. The phase tunable structure of claim 1 wherein the monocrystalline material layer comprises a material selected from the group consisting of: GaAs, AlGaAs, InP, InGaAs, InGaP, ZnSe, and ZnSeS.

25. The phase tunable structure of claim 1 wherein the active device comprises an RF component.

26. The phase tunable structure of claim 25 wherein the electrical device comprises one of a resistor, a capacitor, a diode, a transistor, an integrated logic element, or a CMOS integrated circuit.

27. A phase-shifting structure comprising:

a monocrystalline silicon substrate;

a monocrystalline doped barium strontium titanate (BSTO) layer formed on the substrate, the barium strontium titanate represented as $Ba_zSr_{1-z}TiO_3$, where z ranges from 0 to 1; and

a monocrystalline semiconductor layer formed overlying the BSTO layer.

28. The phase-shifting structure of claim 27 wherein the BSTO layer comprises a composite of BSTO and MgO (magnesium oxide).

29. The phase-shifting structure of claim 27 further comprising an RF component, a DC circuit, and an antenna, wherein the RF component, the DC circuit, and the antenna are each electrically connected to the doped BSTO layer.

30. A phase tunable structure comprising:

a monocrystalline substrate;

a monocrystalline oxide material formed overlying the substrate, the oxide material having phase tunable characteristics; and

a monocrystalline semiconductor material formed overlying the monocrystalline oxide material.

31. The phase tunable structure of claim 30 further comprising a template layer formed between the monocrystalline oxide material and the monocrystalline semiconductor material.

32. The phase tunable structure of claim 30 wherein the monocrystalline oxide material comprises an oxide selected from the group consisting of alkaline earth metal titanates, alkaline earth metal zirconates, alkaline earth metal hafnates, alkaline earth metal tantalates, alkaline earth metal ruthenates, and alkaline earth metal niobates.

33. The phase tunable structure of claim 30 wherein the monocrystalline oxide material comprises $Ba_zSr_{1-z}TiO_3$, where z ranges from 0 to 1.

34. The phase tunable structure of claim 30 wherein the monocrystalline semiconductor material comprises a material selected from the group consisting of: III-V compounds, II-VI compounds, mixed III-V compounds, and mixed II-VI compounds.

35. The phase tunable structure of claim 30 wherein the monocrystalline semiconductor material comprises gallium arsenide.

36. The phase tunable structure of claim 30 further comprising at least one electrical device electrically connected to the monocrystalline oxide material forming an integrated tunable structure.

37. A process for fabricating a phase tunable structure comprising the steps of:

providing a monocrystalline semiconductor substrate comprising silicon;

epitaxially growing a monocrystalline phase tunable oxide layer overlying the monocrystalline substrate; and

epitaxially growing a monocrystalline semiconductor layer overlying the monocrystalline oxide layer.

38. The process of claim 37 further comprising the step of forming a template layer on the monocrystalline phase tunable oxide layer.

39. The process of claim 37 wherein the step of epitaxially growing a monocrystalline phase tunable oxide layer comprises the steps of:

heating the substrate to a temperature between about 400°C and about 600°C; and

introducing reactants comprising strontium, titanium, and oxygen.

40. The process of claim 37 wherein the step of epitaxially growing a monocrystalline semiconductor layer comprises the step of epitaxially growing a layer of gallium arsenide.

41. The process of claim 38 wherein the step of forming a template layer comprises the step of epitaxially growing a surfactant layer.

42. The process of claim 41 further comprising the step of exposing the surfactant layer to form a capping layer.

43. The process of claim 42 wherein the step of exposing comprises exposing the surfactant layer to a halogen.

44. The process of claim 42 wherein the step of exposing comprises exposing the surfactant layer to a halogen selected from the group consisting of As, P, Sb, and N.

45. The process of claim 38 wherein the step of forming a template layer comprises depositing a layer of Zintl type phase material.

46. The process of claim 37 further comprising the step of forming an active device in the monocrystalline semiconductor layer in electrical communication with the monocrystalline phase tunable oxide layer.

47. The process of claim 46 further comprising the steps of:

forming an electrical device at least partially in the monocrystalline semiconductor substrate; and

electrically connecting the electrical device with the monocrystalline phase tunable oxide layer.

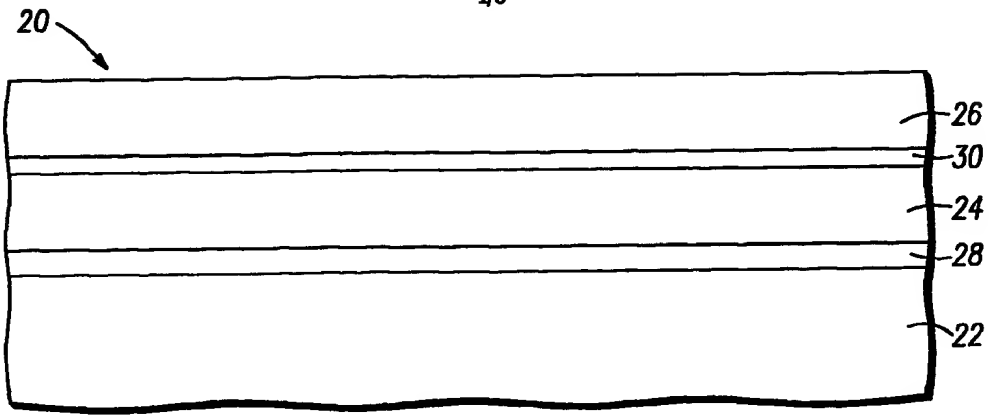

FIG. 1

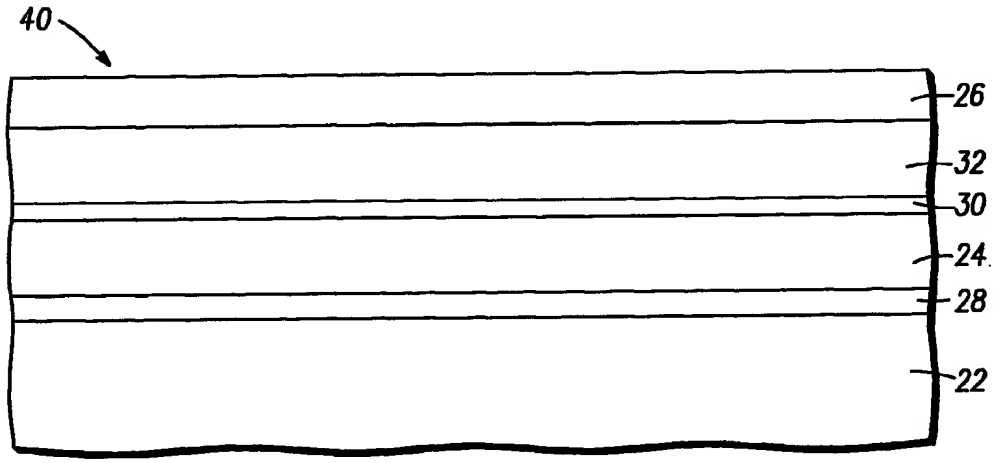

FIG. 2

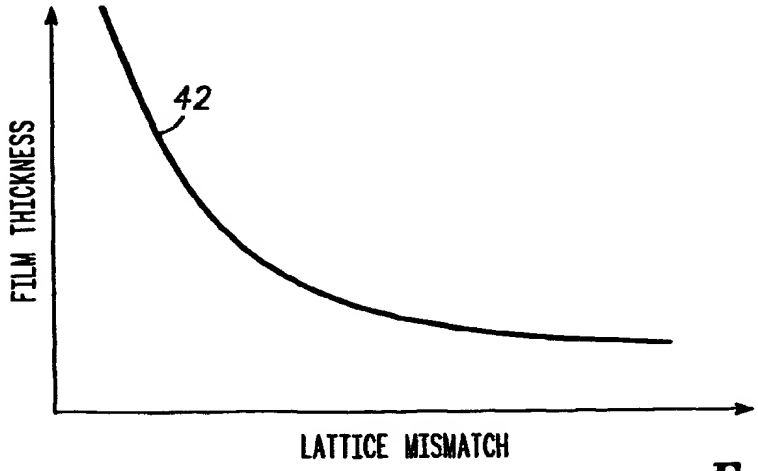

FIG. 3

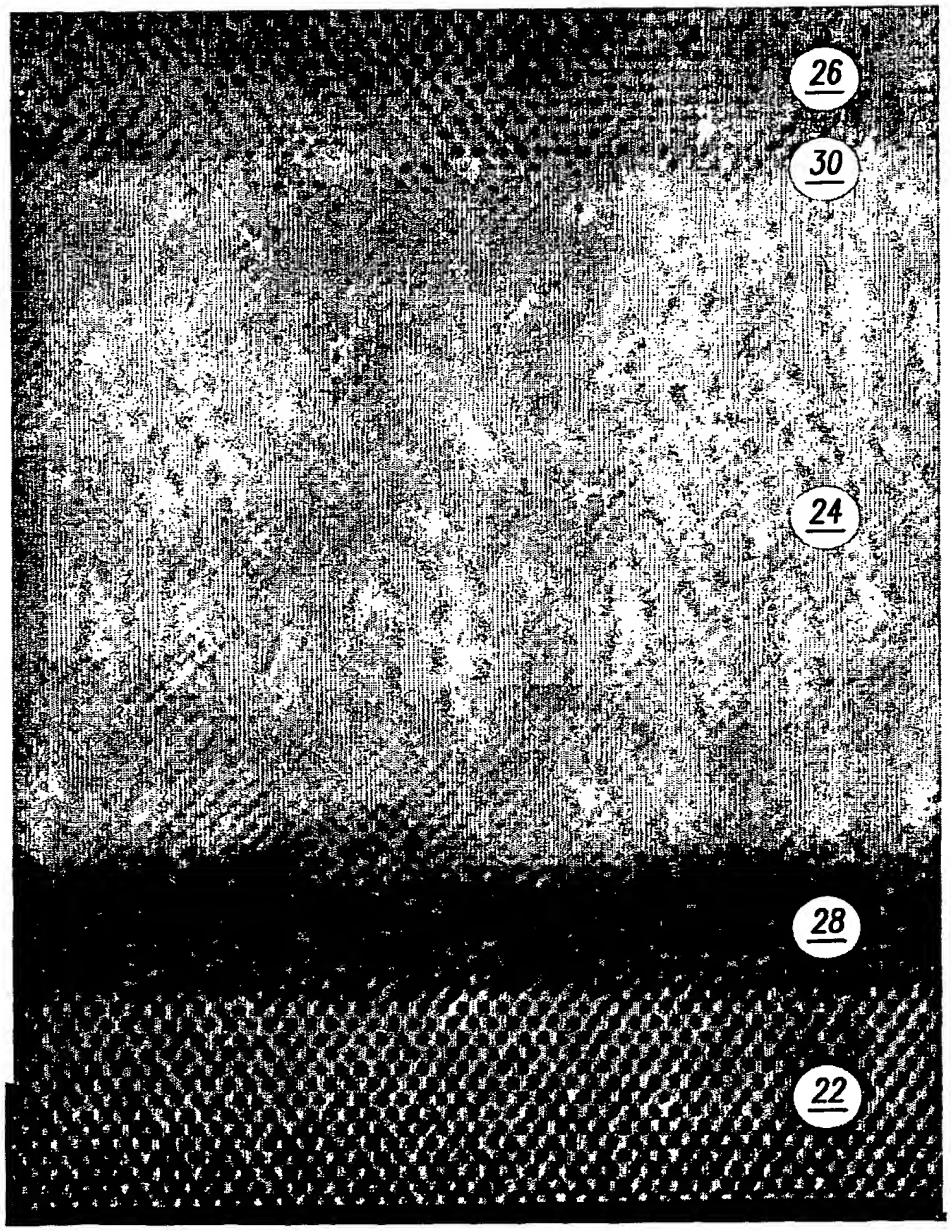

FIG. 4

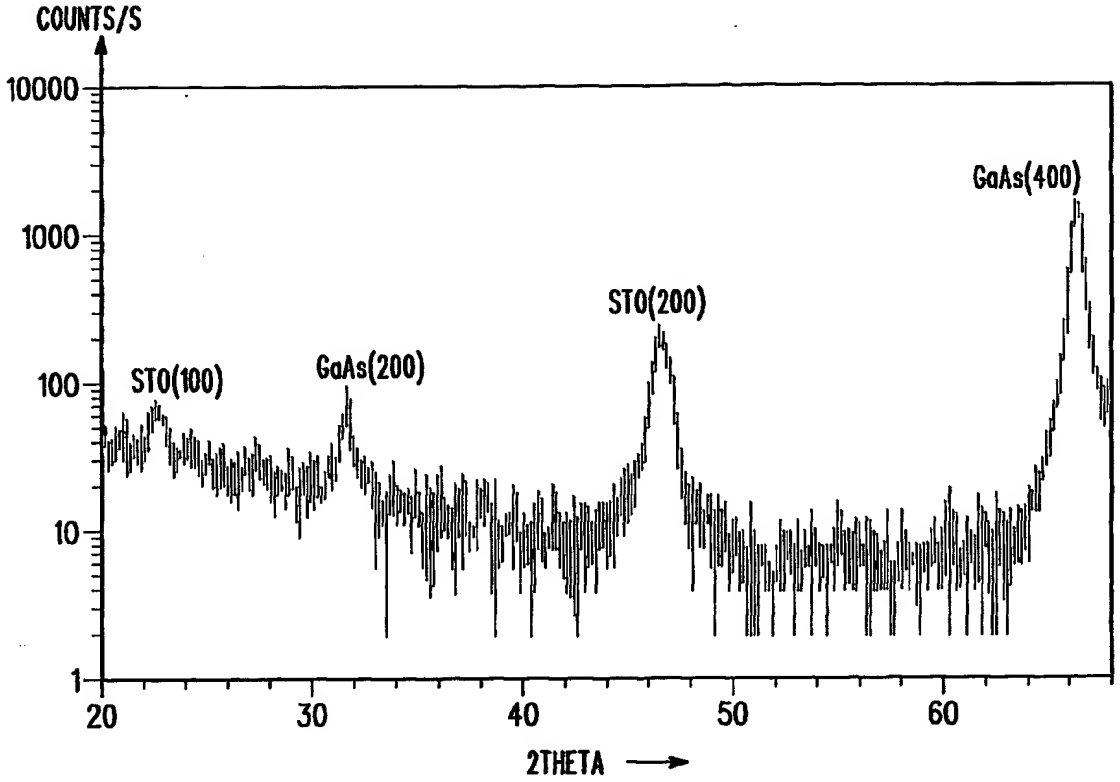
COUNTS/S
10000
1000
100
10
1
STO(100)
GaAs(200)
STO(200)
GaAs(400)
20
30
40
50
60
2THETA

FIG. 5

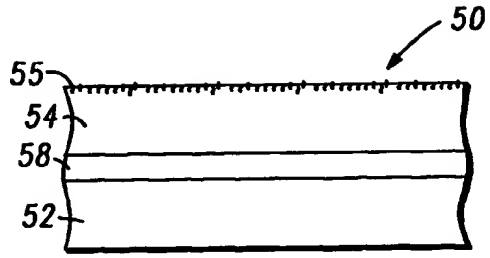

FIG. 6A

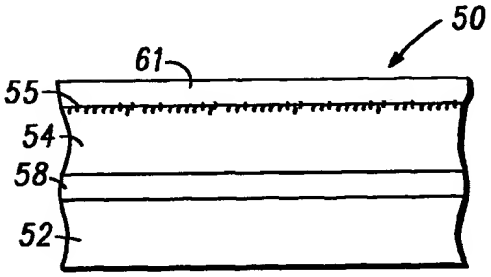

FIG. 6B

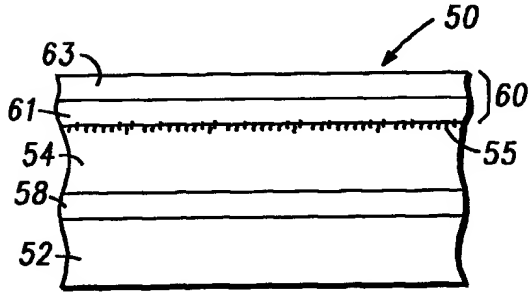

FIG. 6C

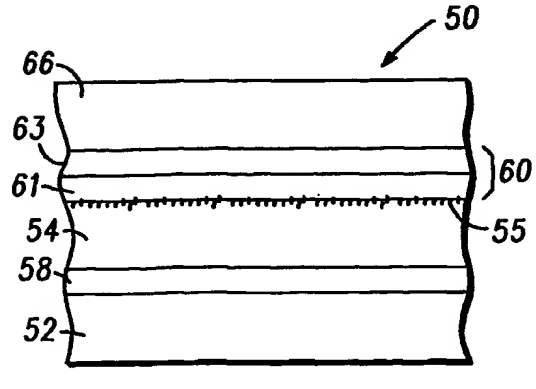

FIG. 6D

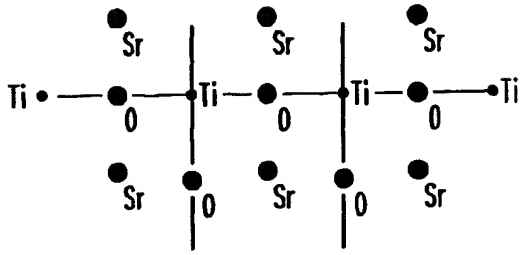

FIG.7A

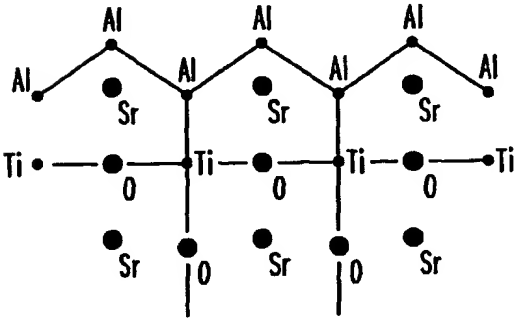

FIG. 7B

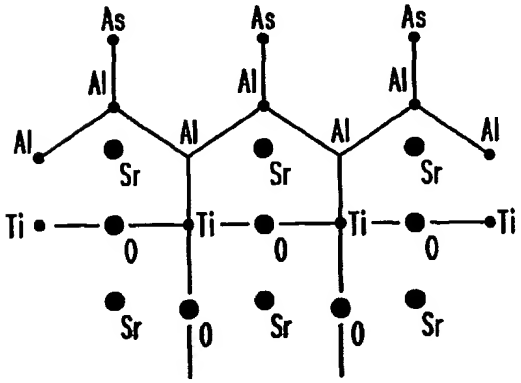

FIG. 7C

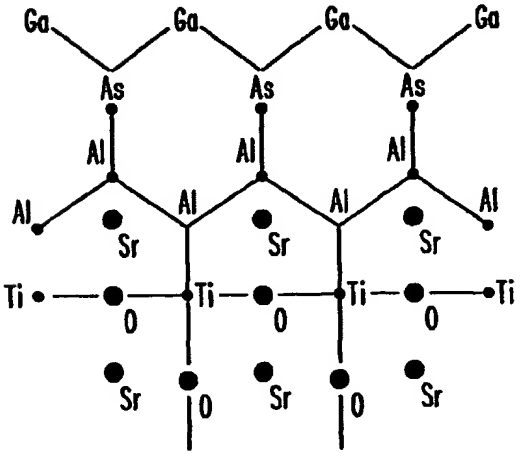

FIG. 7D

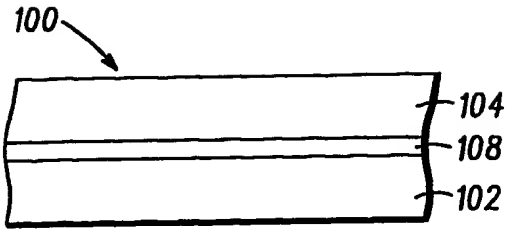

FIG. 8

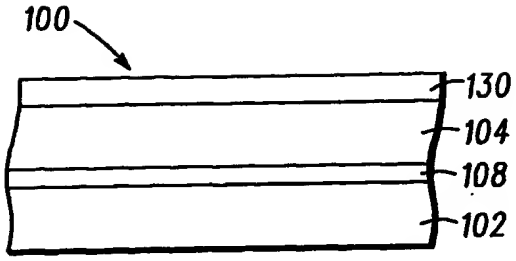

FIG. 9

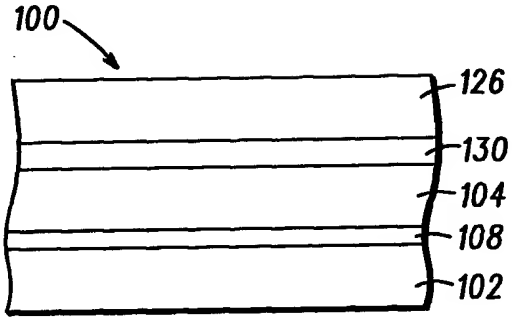

FIG. 10

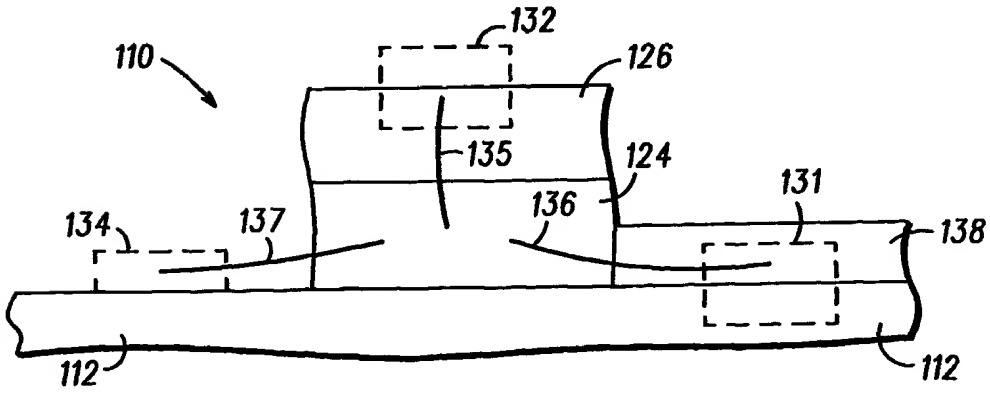

FIG. 11

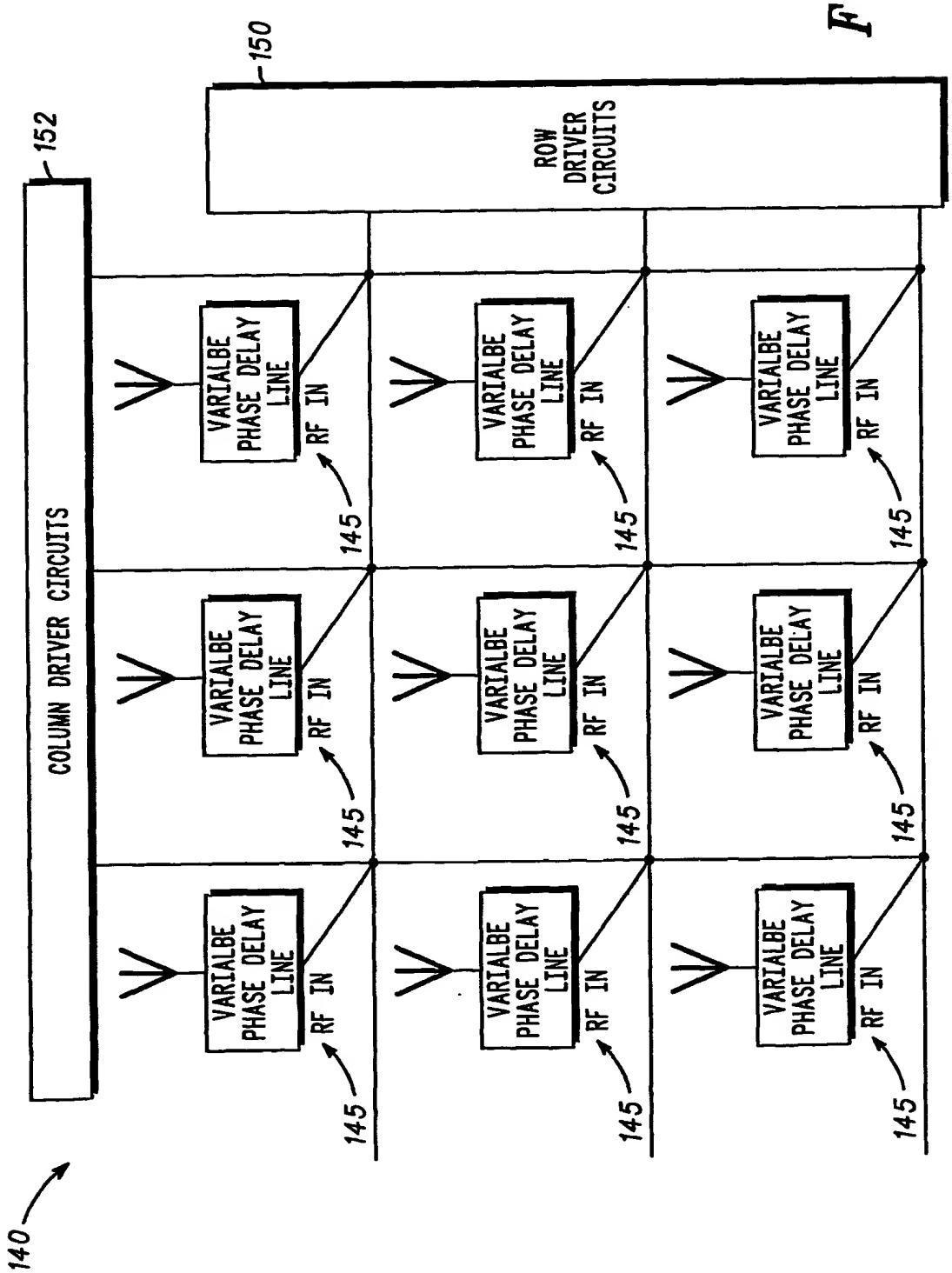
140
152
COLUMN DRIVER CIRCUITS
150
ROW DRIVER CIRCUITS
VARIALBE PHASE DELAY LINE
RF IN
145

FIG. 12